Notice of Allowability	Application No.	Applicant(s)	
	10/616,765	ZHANG ET AL.	
	Examiner	Art Unit	
	Helen B Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 07/02/2004*.

2. ☒ The allowed claim(s) is/are *25-31,65-68 and 73-84*, RENUMBERED (37 CFR 1.126)

3. ☒ The drawings filed on *07/09/2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ANNETTE M. THOMPSON
PRIMARY EXAMINER

DETAILED ACTION

1. This office action is in response to the Application 10/616,765 filed 07/09/2003 and amendment filed 07/02/2004.

2. Claims 25-31, 65-68, 73-84 remain pending in the Application. Claims 1-24, 32-64, 69-72 have been canceled from the Application. Claims 73-84 have been added to the Application.

3. Examiner fully considered Applicant's amendment and finds them persuasive.

Allowable Subject Matter

4. Claims 25-31, 65-68, 73-84 are allowed. The prior art of record does not teach a method of simulating the operation of a circuit, comprising: providing a simulation model of the circuit; selecting a set of frequency points; simulating the response of the circuit for a subset of the frequency points using the simulation model said subset comprising a first group and a distinct second group, wherein each frequency point of said first group lies between a pair of frequency points in said second group of frequency points; interpolating the response of the circuit for the first group of frequency points from the simulated values of the second group of frequency points; comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point; iteratively repeating the interpolating and comparing until the difference between the simulated value and the interpolated value of

each point in the first group do not exceeds the bound; and determining the response of the circuit for frequency points not in the subset from the interpolated response.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chang et al. (US Patent 6,016,623) discloses the interconnect model to determine circuit performance-related characteristics, particularly delay and crosstalk, of interconnects for performance of the method for selecting the minimum number of sampling points with regard to the interline spacing or trace width dimensions wherein during an interactive layout design phase, the capacitance and capacitance derivative of an arbitrarily chosen width and spacing can be interpolated in real time using bi-cubic spline interpolation, but lacks comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point, wherein modeling is for high frequency. Demler (US Patent 6,637,018) discloses the simulation of mixed analog and digital circuitry, determining data points and curve-fitting the data points to determine a model that closely approximates the simulated circuit performance a number of simulations of oscillator frequency for various settings of the design parameters produce simulations for the circuit, but lacks comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the

interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point, wherein modeling is for high frequency using cubic spline interpolation. Glover (US Patent 5,946,211) discloses model to simulate performance of said interconnection path in response to an excitation signal wherein the computer model comprises a subcircuit to simulate he interconnection path, the subcircuit comprising a dc resistance in series with a dc inductance, in parallel with a first frequency resistor in series with a first frequency inductor, said first frequency resistor and inductor series combination having a path to a reference point through a first frequency shunt capacitor, but lacks comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point, wherein modeling is for high frequency using cubic spline interpolation. Liu et al. (US Patent 6,693,439) discloses extracting a model includes extracting a direct current model having direct current model parameters, extracting frequency dependent model parameters, extracting noise data at one or more sampling frequency associating the noise data to at least one bias condition, and extracting a noise model based on the associating and the direct current model parameters. In another exemplary embodiment, simulating the model includes generating a test circuit based on the model and simulating the test circuit but lacks

comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point, wherein modeling is for high frequency using cubic spline interpolation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANNETTE M. THOMPSON
PRIMARY EXAMINER

Examiner
Helen Rossoshek
AU 2825

HR